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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,887	04/06/2001	Hirokatsu Fujiwara	500.39978X00	3367

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TAKEGUCHI, KATHY K

[REDACTED] ART UNIT

[REDACTED] PAPER NUMBER

2187

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DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,887	FUJIWARA ET AL.	
	Examiner	Art Unit	
	Kathy Takeguchi	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 06 April 2001.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,2 and 6-11 is/are rejected.

7) Claim(s) 3-5 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). A certified copy of the priority document has been received.

Claim Objections

2. Claim 6 is objected to because of the following informality:

In Claim 6 (lines 17-18), "memory state information" should be changed to "operating state information" for consistency. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 6-7, and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig et al (United States Patent 6,484,232).

As per Claims 1 and 6:

Olarig teaches an information processing system comprising a memory unit (e.g., Figure 4, element 220) and a memory controller (e.g., Figure 4, element 210), wherein said memory controller includes:

- storing means (*identified as applicants' memory timing table, element 220*) for storing changeable memory control timing information (e.g., Column 9, lines 6-25: The memory controller is programmed to store "the expected life of the memory devices (mean time between failure), the actual life of the memory devices, the error profile for the memory device or module, and any other parameter that may affect the timing of the high speed memory devices, including any user defined parameters");
- monitoring means (*identified as applicants' request issue control circuit, element 21*) for monitoring an operating state of said memory unit (e.g., Abstract, Column 4, line 59-61: "an intelligent memory controller that monitors the immediate environment of the memory devices"; Column 9: The memory controller's control logic "preferably is used to intelligently monitor the remaining useful life of the memory devices, and also to monitor the error history of the memory devices". Additionally, the control logic of the memory controller processes the signals from the sensors. Olarig also suggests that other

implementations and techniques for accurately determining temperature from the multiple sensors may also be used.);

- a register (*identified as applicants' memory control timing register, element 24*) for fetching the memory control timing information from said memory control timing information storing means (e.g., Column 10, lines 48-58: "Error profiles are retrieved by the control logic for a specific memory channel... Information regarding errors, and when they occurred may be stored in a suitable register for recall by the control logic."); and
- control means (*identified as applicants' memory control timing generator circuit, element 23*) for controlling an access timing to said memory unit based on the memory control timing information in said register (e.g., Column 11, lines 7-44) and for changing the information stored in said memory control timing information storing means based on information from said monitoring means (e.g., It is understood that the information relating to the profiles/history are updated based on the monitoring information. Also, refer to Column 9.)

As per Claim 7:

Olarig also teaches a memory controller, wherein:

- said memory unit includes an environmental sensor (e.g., Column 6, lines 28-36), wherein said change control circuit changes said timing information stored in said timing information storing means based on environmental data on said memory unit from said environmental sensor (e.g., Based on the environmental data collected from the sensors, the memory controller adjusts the frequency of the calibration cycles. The frequency of the calibration

cycles affect the operating state of the memory devices, thereby affecting/changing the data generated for the profiles/history.).

As per Claims 10-11:

Olarig also teaches a memory controller, wherein:

- said monitoring means includes a memory fault detector circuit for detecting a fault in a particular group of memory elements to output information indicative of the fault, wherein said change control circuit changes stored timing information corresponding to said group of memory elements in response to the output information from said memory fault detector circuit (e.g., Column 9, lines 6-25; Column 10, line 48 to Column 11, line 19).

Furthermore, it is understood that the fault detected by the fault detector circuit degraded the performance in a particular operation of a group of memory elements.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al (United States Patent 6,484,232).

As per Claim 8:

Olarig teaches the use of sensors, environmental and temperature, for monitoring the state of the memory devices. Although Olarig further teaches that environmental sensors are included to monitor other environmental parameters, “such as humidity, cosmic rays, UV light, vibration, electromagnetic energy, and the like” (e.g., Column 8, lines 30-49), Olarig does not specifically teach that the environmental sensor includes monitoring a current value of said memory unit. However, Olarig further teaches that the “memory controller also is programmed to store...any other parameter that may affect the timing of high speed memory devices, including any user defined parameters” (e.g., Column 9, lines 7-11). Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the teachings of Olarig in order to have the environmental sensor also monitor a current value of the memory unit because tracking the current would allow for the determination of information regarding and related to power dissipation; which affects both the timing and the temperature of the memory unit.

As per Claims 2 and 9:

Olarig teaches storing means (*identified as applicants' memory timing table, element 220*) for storing changeable memory control timing information for the memory device or module (e.g.,

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Column 9, lines 6-25). Olarig further teaches the use of RDRAM to be afforded the advantages of utilizing a special high-speed data bus, the Rambus channel. Yet, Olarig does not specifically teach a memory unit including a mixture of a plurality of groups of memory elements different in operation. However, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to group the RDRAMs or to include a mixture of RDRAMs, different in operation via different data widths (i.e., x4 or x8 or x16), for the purposes of achieving system and clocking requirements.

Furthermore, it would have been obvious to a person having ordinary skill in the art to include a mixture of different types of DRAM other than RDRAM for the purposes of gaining the advantages associated with each type of DRAM. For example, it is well known that DDR SDRAM has relatively high bandwidth, thereby having great speed. Additionally, a mixture of a plurality of groups of memory elements could be utilized for meeting design cost requirements.

Allowable Subject Matter

7. Claims 3-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Conclusion

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- 1) Begin et al (United States Patent 6,173,217)
- 2) Woo et al (United States Patent 6,373,768)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kathy Takeguchi whose telephone number is (703) 305-8115. The examiner can normally be reached on Monday - Friday, 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

KT

Kathy Takeguchi
Art Unit 2187
September 22, 2003

Hiept. Nguyen
HIEPT. NGUYEN
PRIMARY EXAMINER